Amendment to the Claims

Claims 1-12 (Canceled)

13. (Currently Amended) A phase detector for recovering data from a received data signal comprising:

a flip-flop having a data input coupled to a data input port, and a clock input coupled to a clock port;

a latch having a data input coupled to an output of the first flip-flop, and a clock input coupled to the clock port;

a delay element having an input coupled to the data input port;

a first logic circuit having a first input coupled to the output of the flip-flop and a second input coupled to an output of the latch; and

a second logic circuit having a first input coupled to the output of the first flip-flop and a second input coupled to an output of the delay element,

wherein the latch comprises:

first and second MOSFETs having their source terminals connected together, their gate terminals coupled to receive a pair of logic signals, respectively, and their drain terminals connected to a true output and a complementary output, respectively;

a first clocked MOSFET having a drain terminal coupled to the source terminals of the first and second MOSFETs, a gate terminal coupled to receive a first clock signal, and a source terminal;

third and further MOSFETs having their source terminals coupled together, their gate terminals and drain terminals respectively cross-coupled to the true output and the complementary output;

a second clocked MOSFET having a drain terminal coupled to the source of the third and fourth MOSFETs, a gate terminal coupled to receive a second clock signal, and a source terminal;

a first load including a resistive element and an inductive element connected in series and coupling the true output to a first power supply terminal;

a second load including a resistive element and an inductive element connected in series and coupling the true output to the first power supply terminal; and

a current-source MOSFET coupled between the source terminals of the first and second clocked MOSFETs and a second power supply terminal.

14. (Original) The phase detector of claim 13 wherein the first data input port is configured to receive a differential signal.

15. (Original) The phase detector of claim 14 wherein the first clock port is configured to receive a differential signal.

16. (Original) The phase detector of claim 15 wherein the first logic circuit and the second logic circuit are exclusive-OR gates.

17. (Original) The phase detector of claim 15 wherein the first logic circuit and the second logic circuit perform an exclusive-OR function.

18. (Original) The phase detector of claim 13 wherein the first logic circuit provides a reference signal, and the second logic circuit provides an error signal.

19. (Original) An optical receiver comprising the phase detector of claim 13.

20. (Original) An optical transceiver comprising:
an optical transmitter; and
the optical receiver of claim 19 coupled to the optical transmitter.

Claims 21-22 (Canceled)

23. (Previously presented) The phase detector of claim 23 wherein the flip-flop comprises:

a first clocked latch as set forth in claim 23; and

a second clocked latch as set forth in claim 23,

wherein, the gate terminals of the first and second MOSFETs in the second clocked latch respectively couple to the true output and the complementary output of the first clocked latch.